Q.6	i.	Explain the working of CMOS inverter with proper diagram.	**3**
	ii.	Explain the working of TTL Tristate logic with neat and clean diagram.	**7**
OR	iii.	What are the constraints in interfacing TTL with CMOS and vice-versa? Explain with suitable diagrams.	**7**

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Total No. of Questions: 6 *Total No. of Printed Pages:4*

Enrollment No.....

Faculty of Engineering

End Sem (Odd) Examination Dec-2017

CS3ES10 / EC3CO07 / EI3CO07 / IT3ES10

Digital Electronics / Digital Circuit & Systems

Programme: B.Tech. Branch/Specialisation: CS/EC/EI/IT

Duration: 3 Hrs. **Maximum Marks: 60**

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d.

Q.1	i.	Which is the decimal equivalent of largest possible 16 bit binary number? (a) 65536 (b) 65535 (c) 32768 (d) 32767	**1**
	ii.	What should be the Boolean expression for L in Figure 1?	**1**

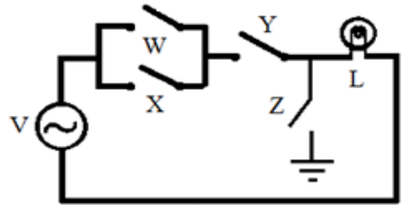

Figure 1

(a) $(W \bullet X)+Y+\overline{Z}$ (b) $(W \bullet X)+\overline{Y} \bullet Z$

(c) $(W+X)+(\overline{Y} \bullet Z)$ (d) $(W+X) \bullet Y \bullet \overline{Z}$

iii. Economically how many 2-input NAND gates are required to implement the Boolean function $Y = \overline{A} \bullet B + C$? **1**

(a) 2 (b) 3 (c) 4 (d) 5

iv. How many inputs a decimal to BCD Encoder should have? **1**

(a) 4 (b) 10 (c) 8 (d) 16

v. In a J-K flip flop the condition $K = \overline{J}$ is used to implement. **1**

(a) D flip flop (b) S-R flip flop

(c) T flip flop (d) Master-slave flip flop

vi. Statement 1: Mealy machine reacts faster to inputs. Statement 2: Moore machine has more circuit delays. Choose the correct option: **1**
(a) Both statements are true
(b) Statement 1 is true but Statement 2 is false
(c) Statement 1 is false and Statement 2 is true
(d) Both statements are false

vii. A Programmable Logic Array consists of **1**
(a) Programmable AND array and fixed OR array
(b) Fixed AND array and programmable OR array
(c) Programmable AND array and programmable OR array
(d) None of these.

viii. If a RAM chip has 12 address input lines then it can access memory locations up to. **1**
(a) 1k (b) 2k (c) 3k (d) 4k

ix. To drive capacitive loads a TTL circuit is modified to have. **1**
(a) Active pull-down element (b) Active pull-up element
(c) Both the elements (d) None of these

x. Which of the following logic family has least power consumption? **1**
(a) DTL (b) TTL (c) RTL (d) CMOS

Q.2 i. A logic circuit implements the following Boolean function. **3**

$$f(w,x,y,z) = \overline{w}\,y + w\,\overline{y}\,\overline{z}$$

It is found that the circuit input combination $w = y = 1$ can never occur. Find a simpler expression for f using proper don't care conditions.

ii. Use K-map to expand the following switching function to canonical SOP form. **7**

$$F(A,B,C) = (\overline{A} + B)(A + B + \overline{C})(\overline{A} + C)$$

OR iii. Use Quine-McCluskey method to minimize the following function. **7**

$$f(w,x,y,z) = \sum m(1,4,7,10,13) + d(5,14,15)$$

Q.3 i. Differentiate between Multiplexer and Demultiplexer. **2**

ii. For the timing diagram shown in Figure 2, find both a minimum NAND and a minimum NOR realization of function $f(A,B,C)$. Use DeMorgan's theorem to show proper Boolean expressions utilized to make such realization. **8**

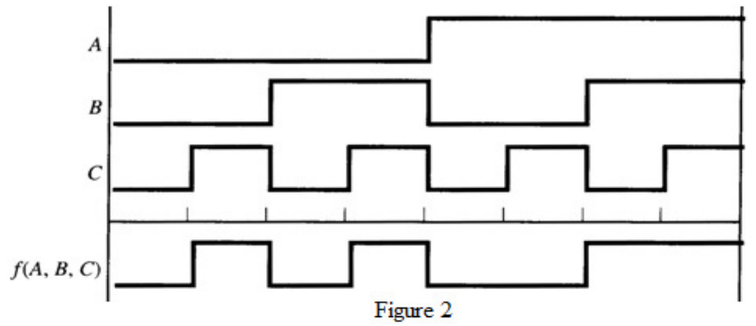

Figure 2

OR iii. Explain and design a BCD to Excess-3 code converter with its block diagram, truth table, expressions and logic diagram. **8**

Q.4 Attempt any two:

i. How S-R flip flop can be converted into J-K flip flop? Explain with the help of excitation table, expressions and logic diagram. **5**

ii. Design a MOD-3 synchronous up counter with the help of state diagram, excitation table, Boolean expressions and logic circuit. **5**

iii. With the help of state diagram, present-next state table expressions and logic diagram design a sequence detector circuit that produces an output '1' whenever an overlapping sequence 101 occurs. **5**

Q.5 i. Differentiate between SRAM and DRAM. **4**

ii. Explain Read Only Memory. Implement the 3-input functions $f_0 = \sum m(0,2,5,7)$, $f_1 = \sum m(1,3,4,6)$ and $f_2 = \sum m(3,4,5)$ using a ROM. **6**

OR iii. Explain PAL with a suitable example. What is its drawback over PLA? **6**

CS3ES10 / EC3CO07 / EI3CO07 / IT3ES10

Digital Electronics / Digital Circuit & Systems

Marking Scheme

Q.1	i.	Which is the decimal equivalent of largest possible 16 bit binary number? (b) 65535	**1**
	ii.	What should be the Boolean expression for L in Figure 1? (d) $(W + X) \bullet Y \bullet \overline{Z}$	**1**
	iii.	Economically how many 2-input NAND gates are required to implement the Boolean function $Y = \overline{A} \bullet B + C$? (c) 4	**1**
	iv.	How many inputs a decimal to BCD Encoder should have? (b) 10	**1**
	v.	In a J-K flip flop the condition $K = \overline{J}$ is used to implement. (a) D flip flop	**1**
	vi.	Statement 1: Mealy machine reacts faster to inputs. Statement 2: Moore machine has more circuit delays. Choose the correct option: (a) Both statements are true	**1**
	vii.	A Programmable Logic Array consists of (c) Programmable AND array and programmable OR array	**1**
	viii.	If a RAM chip has 12 address input lines then it can access memory locations up to. (d) 4k	**1**
	ix.	To drive capacitive loads a TTL circuit is modified to have. (b) Active pull-up element	**1**
	x.	Which of the following logic family has least power consumption? (d) CMOS	**1**
Q.2	i.	For proper don't care form definition – 2 marks For final expression – 1 mark	**3**
	ii.	For correct K-map – 3 marks For proper canonical form (SOP) – 4 marks	**7**
OR	iii.	Table – 1 (No. of 1's) – 1 mark Table – 2 (2 cell combination) – 2 marks Table – 3 (4 cell combination) – 2 marks Table 4 (essential prime implicant) – 1 mark Final exp. – 1 mark	**7**
Q.3	i.	Each proper difference has 1 mark (1 mark * 2 = 2 marks)	**2**
	ii.	Expression of f - 2 marks For each realization- 3 marks. (3 marks * 2 = 6 marks)	**8**
OR	iii.	Block diagram, truth table, expressions and logic diagram - 2 marks each (2 marks * 4 = 8 marks)	**8**
Q.4	i.	Excitation table- 2 marks Expressions- 2 marks Logic diagram- 1 mark.	**5**
	ii.	State diagram- 1 mark State table- 2 marks Expression-1 mark Logic diagram- 1 mark	**5**
	iii.	State diagram- 2 marks State table- 1 mark Expression-1 mark Logic diagram-1 mark.	**5**
Q.5	i.	Each Proper difference has 1 mark (1 mark * 4 = 4 marks)	**4**
	ii.	Definition- 3 marks Function implementation- 1 mark each (1 mark * 3 = 3 marks)	**6**
OR	iii.	Explanation of PAL- 2 marks Example- 2 marks Drawbacks- 2 marks	**6**
Q.6	i.	Diagram- 1 mark Working- 2 marks.	**3**
	ii.	Diagram- 3 marks Working- 4 marks.	**7**
	iii.	Each interfacing has – 3.5 marks with proper diagram & constraints specified (3.5 marks * 2 = 7 marks)	**7**